What is claimed is:

1. A flat panel display, comprising:

a plurality of pixels, each of the plurality of pixels including R, G and B unit pixels to embody red (R), green (G) and blue (B) colors, respectively, each of unit pixels including a transistor with source/drain regions,

wherein transistors of at least two unit pixels of the R, G and B unit pixels have drain regions of different geometric structures.

2. The flat panel display according to claim 1, wherein each of the unit pixels further includes a light emitting device driven by the transistor, and a resistance value of a drain region of the transistor to drive the light emitting device having the highest luminous efficiency of the light emitting devices among the transistors in the unit pixels is higher than those of drain regions of transistors to drive light emitting devices having a relatively low luminous efficiency.

3. The flat panel display according to claim 1, wherein the drain regions of the transistors of the R, G and B unit pixels are of a construction having a same length and a different width from one another, or a construction having a same width and a different length from one another.

4. The flat panel display according to claim 1, wherein the drain regions of the transistors of the R, G and B unit pixels are of zigzag shapes.

5. The flat panel display according to claim 1, wherein each unit pixel further includes a light emitting device driven by the transistor, and a drain region of a transistor to drive the light emitting device having the highest luminous efficiency of the light emitting devices among the transistors in the unit pixels has a longer length or a narrower width compared with

lengths and widths of drain regions of transistors to drive light emitting devices having a relatively lower luminous efficiency.

6. The flat panel display according to claim 1, wherein the drain regions of the transistors of the R, G and B unit pixels include offset regions having different geometric structures from one another, respectively.

7. The flat panel display according to claim 6, wherein each unit pixel further includes a light-emitting device driven by the transistor, and a drain offset region of the transistor to drive the light emitting device having the highest luminous efficiency among the transistors in the unit pixels has a longer length or a narrower width in comparison with lengths and widths of drain offset regions of transistors to drive light emitting devices having a relatively low luminous efficiency.

8. The flat panel display according to claim 1, wherein the drain offset regions of the transistors of the R, G and B unit pixels are of a construction having a same length and a different width from one another, or a construction having a same width and a different length from one another.

9. The flat panel display according to claim 8, wherein the drain offset regions of the transistors of the R, G and B unit pixels are of zigzag shapes.

10. The flat panel display according to claim 1, wherein the unit pixels further include light-emitting devices, respectively, and channel layers of the transistors controlling currents supplied to the light emitting devices of the unit pixels are of same size.

11. A flat panel display, comprising:

a plurality of pixels, where each of the plurality of pixels including R, G and B unit pixels to embody red (R), green (G) and blue (B) colors, respectively, and where each of the unit pixels including a transistor with source/drain regions,

wherein transistors of at least two unit pixels of the R, G and B unit pixels having drain regions of different resistance values.

12. The flat panel display according to claim 11, wherein the unit pixels further include light-emitting devices, respectively, and channel layers of the transistors controlling currents supplied to the light emitting devices of each unit pixel are of same size.

13. The flat panel display according to claim 12, wherein a resistance value of a drain region of the transistor to drive a light emitting device having the highest luminous efficiency among the transistors in the unit pixels is larger than those of drain regions of transistors to drive light emitting devices having a relatively low luminous efficiency.

14. The flat panel display according to claim 11, wherein the drain regions of the R, G and B unit pixels include offset regions having different doping concentrations.

15. The flat panel display according to claim 14, wherein the unit pixels further include light emitting devices driven by the transistors, respectively, and a drain offset region of the transistor to drive a light emitting device having the highest luminous efficiency among the transistors in the unit pixels has a doping concentration lower than those of drain offset regions of transistors to drive light emitting devices having a relatively low luminous efficiency.

16. The flat panel display according to claim 11, wherein the R, G and B unit pixels further include light emitting devices driven by the transistors, respectively, and the source/drain

regions of the transistors include respective offset regions, where the source offset regions of the transistors of the R, G and B unit pixels comprise non-doped regions, and the drain offset regions of the transistors have different impurity doping concentrations in accordance with luminous efficiencies of the light emitting devices.

17. The flat panel display according to claim 11, wherein the R, G and B unit pixels further include light emitting devices driven by the transistors, respectively, and the source/drain regions of the transistors include respective offset regions, where the source offset regions of the transistors of the R, G and B unit pixels comprise regions doped with the same impurity concentration, and the drain offset regions of the transistors have different impurity doping concentrations in accordance with luminous efficiencies of the light emitting devices.

18. The flat panel display according to claim 11, wherein the R, G and B unit pixels further include light emitting devices driven by the transistors, respectively, the source/drain regions of the transistors include respective offset regions, and the source/drain offset regions of the transistors of the R, G and B unit pixels have different impurity concentrations in accordance with luminous efficiencies of the light emitting devices.

19. The flat panel display according to claim 11, wherein at least two transistors of the transistors in the R, G and B unit pixels further include drain offset regions which are doped with impurities having different doping concentrations.

20. The flat panel display according to claim 19, wherein the R, G and B unit pixels further include light emitting devices driven by the transistors, respectively, and a drain offset region of a transistor to drive a light emitting device having the higher luminous efficiency in the

at least two transistors has the doping concentration lower than that of a drain offset region of the other transistor.